UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,140	07/10/2001	Karl-Eugen Kroell	DE9-2000-0026	7994

32074 7590 04/20/2004

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
JONES, HUGH M	

ART UNIT	PAPER NUMBER
2128	10

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 10

Application Number: 09/902,140
Filing Date: July 10, 2001
Appellant(s): KROELL ET AL.

Steven Capella
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/10/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: The double Patenting rejections are withdrawn.

(7) Grouping of Claims

Appellant's brief includes a statement that the claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,442,735	Joshi et al. (PCT search report)	8-2002
4,918,643	Wong (PCT search report)	4-1990
6,063,130	Sakamoto	5-2000

Wong et al. (Appellant's IDS): Accelerated Steady-State Analysis Technique for PWM DC/DC Switching Regulators; IEEE Industrial Electronics, Control and instrumentation, 1996; IECON 97; pp. 759-764 (PCT search report).

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 5, 7, 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

Claims 1-2, 5-8, 13-14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Joshi et al. (US Patent 6,442,735).

Claim 1-2, 5-8, 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

(11) Response to Argument - 102 rejections

The broadest reasonable interpretation has been given to the claims. The Examiner interpreted that static error corresponds to the DC-simulation and that dynamic error corresponds to the transient analysis. The Examiner further interpreted that the transient analysis is also carried out on the same exact circuit and with the same conditions.

The sole issue appears to be as follows. Does a prior art teaching of a determination of whether a simulation of a circuit has *converged* on a *steady state* behavior read on the claimed invention? The Examiner respectfully maintains that it does and maintains the rejections on that sole premise.

The basic argument asserted by Appellants is that the prior art does not disclose or suggest comparing device responses to two different DC conditions. To determine whether circuit behavior has converged to a steady-state *requires a comparison of the same circuit node* over time (different DC conditions cause by the iterative charging or discharging of a circuit element in the previous iteration in the circuit simulation.

Claims 1, 5, 7, 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which ***circuit simulators are able to converge to a steady state solution*** *of a periodic piecewise-linear system or periodically driven piecewise-linear system* transforms the problem into finding the solution of a nonlinear function in terms of a state vector, which is then solved by a truncated power series such as the Newton-Raphson iterative procedure. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

Wong et al. (IEEE - 1997) discloses "*Accelerated* **steady-state analysis** *technique for PWM DC/DC switching regulators.*" Wong et al. further disclose an ***iterative technique for steady-state analysis*** of PWM DC/DC switching regulators.

The algorithm consists of two iteration loops. ***The first one is to iterate the steady-state network waveforms at a presumed duty cycle while the second one is to iterate the steady-state duty cycle of the pulse-width modulator output.*** The circuit waveforms are obtained by a stepwise time domain simulation method, which is based on using stepwise quadratic formulations of the circuit stale variables with progressive analysis of switches' state. *In particular, Wong et al. discloses DC analysis with error detection and correction - see fig.* 2-3 and corresponding text.

Claims 1-2, 5-8, 13-14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Joshi et al. (US Patent 6,442,735).

Joshi et al. disclose a computer program product method of circuit design of a multiple input circuit, macro or chip, especially for silicon on insulator (SOI) circuits. For a multiple input circuit, an object list of items corresponding to circuit devices is created. The items model local effects on corresponding circuit elements. ***The circuit is analyzed using Static or DC analysis to provide initial local effects on circuit devices, including body effects and local heat effects. The initial local effects are passed to the circuit model for transient analysis. The local effects from checked transient results are checked and updated. The transient response is rerun and the local effects are updated until the change in local effects is below an upper limit.*** Note figure 2 and corresponding text, including DC analysis, use of macro and cover models to edit the static error, transient analysis and, again, use of macro and cover model to edit errors.

Claim 1-2, 5-8, 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

Sakamoto discloses: "FIG. 2 is a flowchart illustrating this second prior art. In a step S21, circuit information is input, and in a step S22, a time Tcal for calculating the eigenvalue is read. **In succeeding steps S23 and S24, a circuit matrix is prepared, and a *DC analysis* is carried out.** *In a step S25,* ***a transient analysis is conducted,*** and when the analysis time becomes the time Tcal, matrix data is written into a magnetic disk. After a series of steps (S31 to S36) for the transient analysis are completed, a step S26 for processing the eigenvalue display is conducted. In brief, the matrix data is read out (step S37), and the eigenvalue is calculated on the basis of the read-out matrix data (step S38). A real-number part and an imaginary-number part of the calculated eigenvalue are displayed on an X coordinate axis and a Y coordinate axis, respectively (step S39)."

Thus, Sakamoto discloses a ***steady-state simulation followed by a transient simulation*** (fig. 3 and corresponding text).

Sakamoto does not expressly disclose checking the simulations for errors and then correcting the errors. Wong or Wong et al. disclose checking simulations to ensure accuracy and correcting the simulations when the error is deemed significant.

Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which circuit simulators are able to converge to a steady state solution of a periodic piecewise-linear system or periodically driven piecewise-linear system transforms the

problem into finding the solution of a nonlinear function in terms of a state vector, which is then solved by a truncated power series such as the Newton-Raphson iterative procedure. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

Wong et al. (IEEE - 1997) discloses "*Accelerated steady-state analysis technique for PWM DC/DC switching regulators.*" Wong et al. further disclose an iterative technique for steady-state analysis of PWM DC/DC switching regulators. The algorithm consists of two iteration loops. The first one is to iterate the steady-state network waveforms at a presumed duty cycle while the second one is to iterate the steady-state duty cycle of the pulse-width modulator output. The circuit waveforms are obtained by a stepwise time domain simulation method, which is based on using stepwise quadratic formulations of the circuit state variables with progressive analysis of switches' state. *In particular, Wong et al. discloses DC analysis with error detection and correction - see fig.* 2-3 and corresponding text.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Sakamoto with the teachings of Wong or Wong et al. to obtain the claimed invention for the following reasons. Steady-state and transient simulations are not very useful or realistic if they are not accurate.

In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., that Joshi does not disclose or suggest "performing corrections based on such

comparison of conditions prior to transient analysis") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In general, Appellants still have not addressed the specific sections of the prior art as cited in the Office Action, but have relied on their own interpretation of the cited prior art.

In response to appellant's argument relating to Wong ('643 patent), it is noted that the sections, as indicated by Appellants (page 6, paper # 4) do not appear to disclose the alleged features as argued by Appellants. In any case the indicated col. 2, refers to "background" teachings. Appellants are silent with respect to the sections of the patent as directed by the Examiner. Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which circuit simulators are able to converge to a steady state solution of a periodic piecewise-linear system or periodically driven piecewise-linear system transforms the problem into finding the solution of a nonlinear function in terms of a state vector, which is then solved by a truncated power series such as the Newton-Raphson iterative procedure. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

In response to arguments relating to Wong (IEEE), Appellants are, again, silent as to the sections of the applied prior art which were indicated in the rejection. *Wong et*

al. discloses DC analysis with error detection and correction - see fig. 2-3 and corresponding text.

In response to arguments relating to Joshi, Appellants silent as to the cited sections, recited in the last office action. Joshi et al. disclose a computer program product method of circuit design of a multiple input circuit, macro or chip, especially for silicon on insulator (SOI) circuits. For a multiple input circuit, an object list of items corresponding to circuit devices is created. The items model local effects on corresponding circuit elements. ***The circuit is analyzed using Static or DC analysis to provide initial local effects on circuit devices, including body effects and local heat effects. The initial local effects are passed to the circuit model for transient analysis. The local effects from checked transient results are checked and updated. The transient response is rerun and the local effects are updated until the change in local effects is below an upper limit***. Note figure 2 and corresponding text, including DC analysis, use of macro and cover models to edit the static error, transient analysis and, again, use of macro and cover model to edit errors.

In response to arguments relating to Sakamoto (103 rejections), Appellants are, again, silent as to the sections of the applied prior art which were indicated in the rejection. Appellant's arguments do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Appellants arguments again rely on their arguments against the 102 rejections and are not persuasive for the same reasons. Furthermore, in response to appellant's arguments against the references individually,

one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In summary, the sole issue appears to be as follows. *Does a prior art teaching of a determination of whether a simulation of a circuit has converged on a steady state behavior read on the claimed invention?* The Examiner respectfully maintains that it does and maintains the rejections on that sole premise.

The basic argument asserted by Appellants is that the prior art does not disclose or suggest comparing device responses to two different DC conditions. To determine whether circuit behavior has converged to a steady-state *requires a comparison of the same circuit node* over time (different DC conditions cause by the iterative charging or discharging of a circuit element in the previous iteration in the circuit simulation.

A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hugh Jones
Primary Examiner
April 18, 2004

Conferees
Kevin Teska (SPE)
William Thomson (Primary Examiner)

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

HUGH JONES PH.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100